IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of:	]
OLIVIER MARTY et al	]
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Serial No: 10/512,077	]
	]Group Art Unit: 1792
	]
Filed: December 9, 2004	]Examiner: G. Rao
	]
For: PROCESS FOR MODIFYING THE PROPERTIES OF A THIN LAYER AND SUBSTRATE APPLYING SAID PROCESS	]Attorney Docket: 04202
	]

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Universite Claude Bernard Lyon I, Villeurbanne, France.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 17-27 are currently pending, and are rejected and under appeal.

Claims 1-16 have been canceled.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is directed to a process for forming a

substrate to be utilized in microelectronics, nanoelectronics, microtechnology or nanotechnology (page 8, lines 26-28) comprising a support (2; page 10, lines 12) having a thin layer (1; page 10, line 6) formed on an upper surface thereof, comprising the steps of:

forming at least one said thin layer on the upper surface of a nanostructured support (page 13, line 8- page 14, line 2), and subsequently

treating the nanostructured support to generate internal strains in the support, causing deformation of the support by dilation or contraction at least in the plane of the thin layer, so as to ensure a corresponding deformation of the thin layer and modification of properties of the thin layer (page 14, lines 4-15).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Whether claims 17-24 are anticipated under 35 USC 102(b) by JP 2000-91627 to Yoshida.

2) Whether claims 25-27 are obvious under 35 USC 103(a) over JP 2000-91627 to Yoshida in view of US 6,365,059 to Pechenik.

VII. ARGUMENT

The invention relates to a method for forming a substrate which can be utilized in microelectronics, nanoelectronics, microtechnology or nanotechnology, and which comprises 1) a nanostructured support having 2) a thin layer thereon. According to the claimed method, a thin layer is deposited on the nanostructured support, and the nanostructured support is subsequently treated to generate internal strains therein, and to cause deformation in the support by dilation or contraction, the deformation being situated in the plane of the thin layer. This deformation in

the plane of the thin layer causes a corresponding deformation of the thin layer.

In any event, it is clear that claim 17 requires 1) deposition of the thin layer, followed by 2) a treatment of the support by dilation or contraction, and 3) a corresponding deformation of the thin layer which occurs as a result.

The thin layer must be of sufficiently small thickness that the layer remains elastic in nature, and the deformation does not cause structural defects such as dislocations or cracking in the substrate.

Yoshida is directed to a light emitting device comprising a glass substrate, a lower tungsten electrode, a GaP thin film (13) which is 300 nm in thickness (an isoelectronic trap), and an upper transparent electrode made of thin indium oxide (ITO). The process disclosed by Yoshida involves the formation of the isoelectronic trap by sputter deposition, which allows the formation of a polycrystalline GaP doped with N_2 on the upper tungsten layer (32). Immediately after this deposition and before the formation of the top transparent electrode, a radiation treatment is performed to promote a surface lattice rearrangement. By this heat treatment, which results in an increase in particle diameter and removal of the non-radiating recombination center near the grain boundary, the semiconductor membrane (33) is reformed to the semiconductor membrane active layer (34) as a light emitting device.

This heating step is described in paragraph [0013] of the machine translation:

> In a manufacturing method of a light emitting device and a display device of this invention, afer depositing the

> easiest crystalline member, such as polycrystal or an amorphous substance, radiation heating is performed and the crystallinity of said semiconductor membrane is changed.

With respect to Yoshida, the Office Action of July 3, 2008 makes the following argument:

> Yoshida '627 pertains to the fabrication of a semiconductor LED whereby the substrate and thin layer formed atop are in the nanoscopic scale, thus defining them as nanostructured materials and providing for their utilization in a field such as microelectronics or nanotechnology. Whereby the thin layer is disposed on the substrate via an epitaxial deposition (such as MBE or MOCVD), followed by the radiation heat treatment which in part affects the substrate in order to aid in the heteroepitaxial adherence between the two materials, forcing the substrate to incur internal dislocations, which would inherently result from an initial dilation and contraction of the substrate as a result of the treatment which in turn would effect the thin film but ultimately allow for the two materials to adhere much more strongly to one another.

What is important here is that Yoshida teaches *a heat treatment of the thin layer*, and *not a heat treatment of the support*. The Office Action appears to admit this, but then goes on to make the allegation that the heat treatment affects the substrate in order to aid heteroepitaxial adherence between the materials, which causes dislocations in the substrate, which affects the thin film.

In other words: Even though the invention is directed to treating the substrate and the reference teaches treating the thin film, the invention is still anticipated because

treating the thin film causes dislocations in the substrate, causing the desired deformation in the thin film.

The problem is that the position taken in the Office Action is based upon speculation, and is not supported by any specific citation in the Office Action. Appellants' position is that the treatment which recrystallizes the semiconductor membrane has no effect on the support whatever, and the Office Action has presented no evidence to the contrary. What is taught by Yoshida is recrystallization of a layer which does not correspond to the elastic deformation of the support according to the invention. Any allegation that this occurs in the teaching of Yoshida is unsupported.

Moreover, Yoshida does not teach one how to obtain the elastic deformation according to the invention because the purpose of Yoshida is to recrystallize a material to increase its optoelectronic properties. There is no suggestion in Yoshida of how to make a layer with a lattice parameter adapted to the material to be formed thereafter by epitaxial growth.

The Office Action makes the further argument that:

> As discussed before the process for fabrication of the nanostructured device the formation of the thin layer on the nano-structured support, the internal strains that result, and the dilation or contraction of the "substrate" will inherently occur as a result of the heteroepitaxial layering process of the thin film deposited over the nanostructured substrate. Furthermore Yoshida '627 requires the use of MBE or MOCVD for deposition, which generally occur in reaction chambers that require temperature and pressure changes, two factors known to affect a materials property via transition of the DBTT (Ductile-Brittle Transition Temperature)

> rule, and therefore would inherently result in the substrate dilating or contracting in response to the temperature, pressure, and chemical changes resulting from the deposition process.

In other words: The process of depositing the crystalline material in itself causes deformation of the substrate.

This allegation is also unsupported, but even if true would not result in anticipation of the claimed invention, since the invention requires the treatment of the substrate causing dislocations only after the thin layer has been deposited on the upper surface. The interpretation made in the Office Action permits disregards the second claimed step of the invention, "treating the nanostructured support..." because it may be inherent in the first step.

To summarize, claim 17 recites a two step process of depositing a thin layer on a support, and *subsequently* treating the support to generate internal strains in the support which are also in the plane of the thin layer, and thereby cause a corresponding deformation of the thin layer.

Under no interpretation of Yoshida can these steps as defined be said to be taught. Yoshida teaches depositing a thin layer on a support, but then teaches radiation heating to recrystallize the thin layer; no treatment of the support is either disclosed or suggested. Any argument that a treatment of the support occurs either explicitly or inherently is based entirely on speculation.

With respect to claims 25-27, Pechenik has been cited for a teaching of the use of piezoelectric thin films in nano-based devices. Pechenik, however, does not cure the

defects of Yoshida, and specifically does not disclose or suggest dilation or contraction of a support in order to obtain a corresponding dilation or contraction of a thin layer on the support.

Reversal of the rejections of record is requested.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

17. A process for forming a substrate to be utilized in microelectronics, nanoelectronics, microtechnology or nanotechnology comprising a support having a thin layer formed on an upper surface thereof, comprising the steps of:

forming at least one said thin layer on the upper surface of a nanostructured support, and subsequently

treating the nanostructured support to generate internal strains in the support, causing deformation of the support by dilation or contraction at least in the plane of the thin layer, so as to ensure a corresponding deformation of the thin layer and modification of properties of the thin layer.

18. The process as claimed in Claim 17, wherein the treating comprises treating the nanostructured support chemically to cause deformation of the nanostructure thereof.

19. The process as claimed in Claim 17, wherein the nanostructured support is selected from the group consisting of a metals, semi-conductors and dielectric materials.

20. The process as claimed in Claim 17, additionally comprising effecting the epitaxial growth of a crystalline material on the thin layer, after the treating.

21. The process as claimed in Claim 20, wherein the thin layer is selected to be capable of possessing a lattice parameter corresponding to a lattice parameter of a crystalline material to be formed by said epitaxial growth.

22. The process as claimed in Claim 21, wherein the thin layer is prestrained.

23. The process as claimed in Claim 17, additionally comprising forming on the nanostructured support at least one intermediate layer disposed between the thin layer and the nanostructured support.

24. The process as claimed in Claim 20, wherein the crystalline material is semi-conductor or superconductor material.

25. The process as claimed in Claim 17, wherein the thin layer is made of a material having piezoelectric properties.

26. The process as claimed in Claim 25, additionally comprising performing a lithographic operation on the thin layer to reveal piezoelectric zones.

27. The process as claimed in Claim 25, additionally comprising deforming the nanostructured support so that electrical charges appear in the thin layer.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.